

LT24102

Auto-Configuration - Five Way 16/8 lane PCIe Gen 2.0 SoC



HYDRALOGIX 200 Series

Lucid's next generation silicon, the LT24102, is a SoC device providing a generic multi GPU solution for motherboard and AIB vendors. The LT24102 is a unique PCIe Gen2 device designed to scale graphic performance in a multi GPU environment.



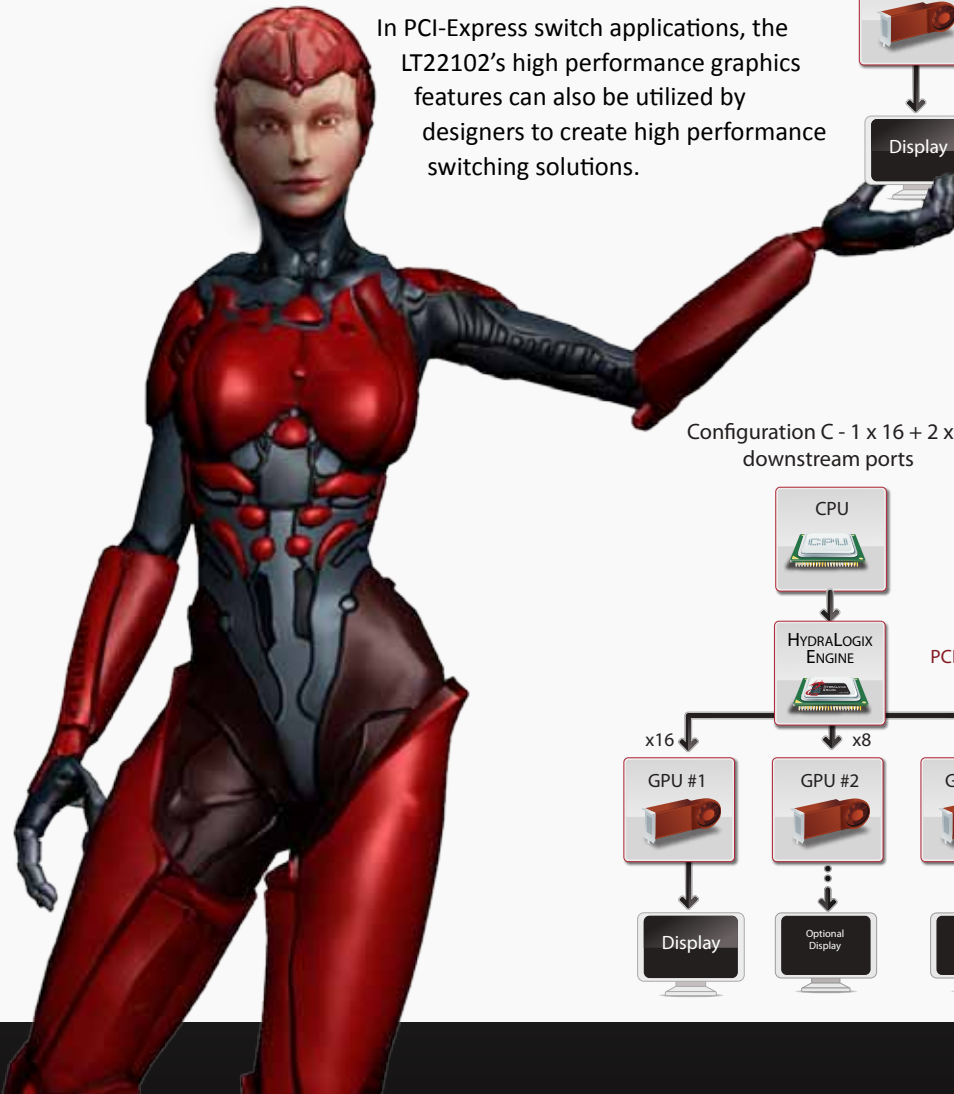
HYDRALOGIX 200

The LT24102

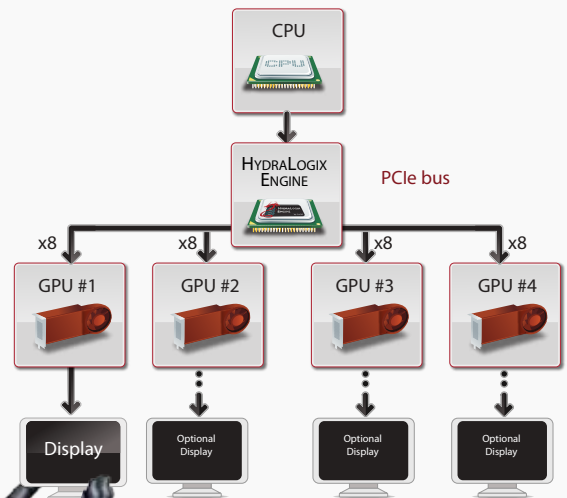
The device incorporates 48 5 Gbps SERDES lanes, a full PCI-Express switch with one x16 upstream port, two x16 or four x8 downstream ports and an embedded end point. The upstream port is typically connected to the system's chipset (North Bridge) or directly to the Host CPU. Any of the four downstream ports can be connected to any GPU, up to four GPUs from any vendor can be connected in any order. The embedded end point incorporates a RISC processor and DMA engines used by Lucid's proprietary algorithms.

The LT24102 connects seamlessly to any vendor's chipset or CPU that comprises a Root Complex, and to any vendor's GPU. It is fully compliant with Microsoft Vista, Win7 OS and DirectX 9, DirectX 10, and DirectX 11 standard APIs. Together with the unique HYDRALOGIX driver, the LT24102 provides an adaptive and dynamic, parallel graphics load-balancing scheme, which resolves bottlenecks in the system and optimizes the usage of GPU resources with minimal power consumption.

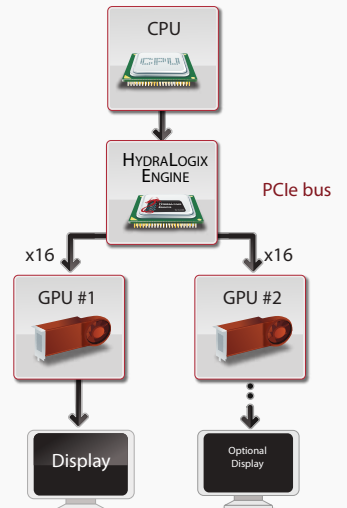
In PCI-Express switch applications, the LT24102's high performance graphics features can also be utilized by designers to create high performance switching solutions.



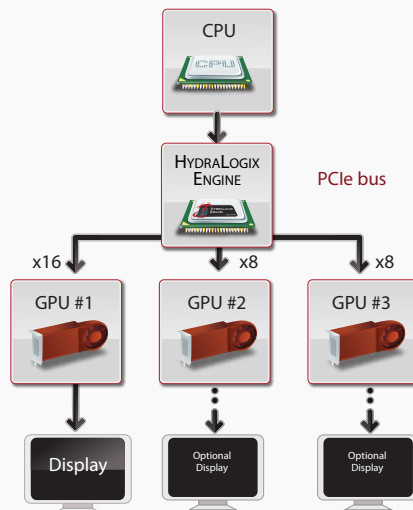
Configuration B - 4 x 8 downstream ports



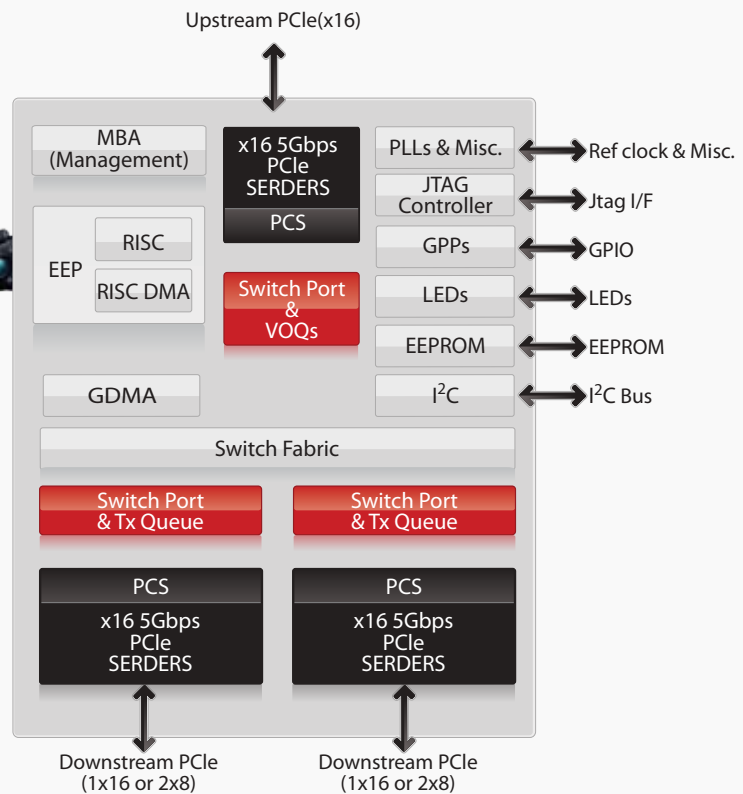
Configuration A - 2 x 16 downstream ports



Configuration C - 1 x 16 + 2 x 8 downstream ports



LT24102 block diagram



FEATURES

PCI EXPRESS INTERFACES

- PCI Express 2.0 compliant. Backward compatible with PCI Express 1.2a
- 48 lanes of 5 Gbps SERDES
- One x16 upstream port
- Two x16 or one x16 and two x8 or four x8 downstream port (Auto-configuration)
- Lane reversal on all ports
- Supports PCI Power Management Interface specification
- Unused SERDES are disabled to save power
- Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state

PCI EXPRESS SWITCH PORT

- Up to five PCI Express switch ports
- Fully Compliant with PCI Express logical protocol layers, Data Link Layer and Transaction Layer
- One virtual channel
- Eight Traffic Classes
- Maximum payload size of 256B
- Legacy PCI INTx emulation
- MSI Support
- Support for PCI Express Advanced Error Logging

EMBEDDED RISC

- Tensilica Diamond Architecture 32-bit RISC
- 300 Mhz clock
- 64 Kbytes on-chip instruction memory
- 32 KBytes on-chip data memory
- On chip DMA engine to enable PCIe packet generation and reception
- Real time control over the switch operation

OTHER

- 483 FCBGA 23 x 23 mm package with 1 mm pitch
- Two LED outputs per PCIe interface
- Jtag Interface with AC and DC JTAG Support
- Optional four wire EEPROM interface
- Optional I²C bus
- Single 100 Mhz reference clock
- Power consumption: 6 Watts

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