

Open-Silicon, Inc. Tapes Out High Lane Count SerDes Designs

MILPITAS, Calif.-January 28, 2009: Open-Silicon, Inc., the leading open market semiconductor manufacturer and provider of spec-to-silicon ASIC design services, today announced successful completion of two complex ASIC designs. The designs, which included large numbers of integrated high-speed serializer/deserializer (SerDes) cores, demonstrate Open-Silicon's high-end digital IC design capabilities and ability to integrate complex open market IP. While Open-Silicon has worked on a total of 30 ASICs with SerDes to date, the high lane count of these two recently completed devices made them particularly challenging in the areas of timing closure, package design, test, and physical design for signal integrity.

The first chip, which is not yet announced, integrated over 50 SerDes for a networking application. An additional challenge was imposed by the addition of high speed DDR2 interfaces. To handle all the high-speed IO requirements this chip was packaged in a custom HFCBGA package.

The second of the chips is a Parallel Graphics Unit for gaming and computing designed with LucidLogix Technologies. This ASIC serves as a scalable graphics component connecting a main computer processor to multiple GPUs. A 12-quad 48-channel 2.5Gbps PCIe SerDes network is used to divide graphics processing work among several graphical processing units (GPUs). On this device the PCI Express lanes were spread evenly on all four sides of the die to facilitate use of low-cost wirebond packaging. As a single reference clock feeds all 48 lanes, a novel clock buffer ring was built outside the chip's bond pads to isolate the clock from on-chip noise. Due to the high numbers of SerDes lanes, both designs required careful attention to:

1. Co-design of custom package with die physical design
2. Physical design taking into account the macro placements and signal interactions at very high speeds
3. Extensive SPICE level analysis of critical paths to analyze timing and cross-talk for the large number of SerDes lanes
4. Careful design of power sources to bring power to the macros
5. Verification early in the design phase that the SerDes DFT structures and Automated Test Equipment (ATE) will be able to provide complete and accurate test for production

"High-end 3D graphics processing depends on silicon solutions that require a high degree of design expertise," said Offir Remez, President and Vice President of Business Development for Lucid Information Technologies. "The Open-Silicon design team tackled our tough chip requirements and met our specifications."

About Open-Silicon

Open-Silicon, Inc. is a fabless ASIC company that was founded to set new standards for the predictability and reliability of ASICs and enable customers to differentiate their products through affordable custom silicon. Open-Silicon provides leading edge ASIC design, open market IP integration, and high quality silicon manufacturing services to customers worldwide. Through the "Science of ASICs" initiative Open-Silicon continues to introduce technology advantages that help customers increase their market success. For more information, visit Open-Silicon's website at www.open-silicon.com or call 408-240-5700.

About Lucid

LucidLogix Technologies is reinventing multi-core graphics with its HYDRA real-time distributed processing engine that will exponentially improve visual computing for both business and gaming applications. Lucid is a fabless SoC provider headquartered in Kfar Netter, Israel. For more information, visit www.lucidlogix.com.

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